REMARKS

In the Office Action of July 3, 2008, all of the claims were rejected under 35 U.S.C. § 103 as unpatentable over Joy et al. (USP 4,454,647) in view of Lee et al. (US 2002/0076879). Applicants respectfully traverse the rejections.

Joy et al. addresses the bird's beak problem of the prior art. The purpose of the embodiments disclosed in Joy et al. is to provide a smooth abutting silicone dioxide surface. Joy et al. discusses the bird's beak problem in the "Description of the Prior Art" section.

> The final consequence of this is a general stress in the perimeter region of the groove as well as difficulties in subsequently achieving good abutted diffusions against the vertical portion of the silicon dioxide. This nonabutting capability defeats to some extent a major benefit of the original purpose of the silicon dioxide region. Joy et al., col. 1, lns. 59-64.

The "Summary of the Present Invention" section of Joy et al. explains the achievement of the disclosed embodiments as follows:

> The isolation structure provided herein allows for the abutting of the subcollector, extrinsic base, emitter, and resistor junctions, etc., to dielectric material. The abutting of junctions reduces the total junction area required which in turn reduces the capacitance associated with each device, thereby, improving performance. In addition the distance between devices can be reduced leading to increased circuit density and improved performance. (Joy et al., col 3, lns. 45-53)

Referring to FIG. 4 of Joy et al., in light of the description protrusions above the silicon dioxide layer 32 are not desirable, and in fact, would be contrary to the purpose of providing an abuttable surface. Thus, Lee et al., having a silicone dioxide layer 35 protruding above the surface of the substrate 10, is not combinable with Joy et al. as is stated in the Office Action. In sum, Joy et al. teaches against having a protruding silicone dioxide layer 35.

In addition to the above, Applicants wish to point out that the motivation stated in the Office Action for combining Lee et al. with Joy et al. is not due to having a second insulating layer on top of the conductive plug. Lee et al. states that its

achievement of "tight device isolation" and reducing "the occurrence of the inverse narrow width effect" is attributable to a conductive plug in a trench isolation structure. Lee et al. explains in ¶ 24:

> Embodiments of the present invention will now be described in detail below with reference to FIGS. 4 through 15, which illustrate various embodiments of the present invention, and various processes of fabricating embodiments of the present invention. In embodiments of the present invention, **an integrated circuit device is provided that includes a conductive plug in a trench isolation structure that is electrically connected to the substrate through a trench floor that is at least partially devoid of an insulating layer.** In other embodiments of the present invention, the trench floor may be completely or substantially devoid of an insulating layer. Thus, if a substrate is lightly doped with P-type impurities, the conductive plug and the substrate may form an ohmic contact. Therefore, a voltage applied to the substrate may be directly applied to the conductive plug in the trench making it is possible to achieve tight device isolation between the active regions having a source/drain region that is doped with n-type impurities. **Thus, the present invention may reduce the occurrence of the inverse narrow width effect.** (bold added)

Nowhere in this paragraph does Lee et al. mention any benefit of having the silicone dioxide layer 35 protrude above the surface of the substrate 10. Also, this paragraph does not attribute a reduction in the occurrence of the inverse narrow width effect to a silicone dioxide layer above the surface of the substrate. In fact, the protrusion feature of Lee et al. is discussed in ¶ 28 and does not mention any benefit thereof:

> [0028] A second insulating layer is provided on the top of the conductive plug. The second insulating layer may include, for example, a silicon nitride layer 33. The silicon nitride layer 33 may have a thickness from about 10 .ANG. to about 500 .ANG.. The second insulating layer may further include a layer of silicon oxide 35. As illustrated in FIG. 5, the second insulating layer is on the plug top 50 and may extend onto the trench sidewall 45 between the plug top 50 and the face 40 of the substrate 10. Alternatively, the second insulating layer may include a conformal insulating layer on the plug top 50 that

is recessed beneath the face 40 of the substrate 10 and also extends onto the trench sidewall 45 between the plug top 50 and the face 40 of the substrate 10. A chemical vapor deposition (CVD) silicon oxide layer may optionally be provided on the surface of the integrated circuit device (not shown).

For at least the reasons stated above, Applicants respectfully request that the obviousness rejection be withdrawn. Claim 1-6 are believed allowable.

New Claims 15 and 16

New Claim 15 provides:

15. The semiconductor component of claim 1, wherein the trench contact includes:

a trench contact insulation layer above a surface of the electrically conductive filling layer; and

a contact opening through the trench contact insulation layer and in contact with the surface of the electrically conductive filling layer.

Support for Claim 15 is at least shown in FIG. 1N and discussed at least in ¶'s 35 and 38 of the present application. Neither Joy et al. nor Lee et al. disclose the contact opening as claimed. Claim 15 is believed allowable.

New Claim 16 provides:

16. The semiconductor component of claim 1, further comprising a gate oxide layer over a surface of the second covering insulation layer.

Support for Claim 16 is at least shown in FIG. 1N and discussed at least in ¶ 38 of the present application. Neither Joy et al. nor Lee et al. disclose a gate oxide layer over a surface of the second covering insulation layer. Claim 16 is believed allowable.

Applicants respectfully request the allowance of claims 1-6, 15, and 16.

CONCLUSION

Therefore, in view of the above remarks, we respectfully submit that this application is in condition for allowance and such action is earnestly requested.

If for any reason the Examiner is not able to allow the application, he is requested to contact the Applicants' undersigned attorney at (312) 321-4200.

Date: September 3, 2008

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